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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: John Wynne et al
Patent No.: 6,924,759
Issued: AUG 15 2005 August 2, 2005
Serial No.: 10/731,334
Confirmation No.: 5008
Filed: December 9, 2003

For: MULTI-CHANNEL INTEGRATED CIRCUIT COMPRISING A PLURALITY OF DACs, AND A METHOD FOR MONITORING THE OUTPUT OF THE DACs

Examiner: Lam T. Mai
Art Unit: 2819

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop Certificate of Correction, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 11th day of August, 2005.



Steven J. Henry
Reg. No. 27,900

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P.O. Box 1450
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Certificate
AUG 17 2005
of Correction

Sir:

Transmitted herewith are the following documents:

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If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646-8000, Boston, Massachusetts.

No check is enclosed to cover the fees. If the fee is insufficient, the balance may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

Respectfully submitted,



Docket No.: G0631.70032 US01
Date: August 11, 2005

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Alexandria, VA 22313-1450

Sir:

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. §1.322

Patentee's Assignee respectfully requests the correction of errors found in the printing of the above-captioned patent. The requested corrections rectify typographical errors made by the Patent and Trademark Office.

The corrections requested do not involve a change in the patent that constitutes new matter or would require reexamination. Therefore, Patentee's Assignee requests that a certificate of correction be issued. A copy of the first page of the pertinent issued patent with the errors highlighted is enclosed.

No fee is required under 37 CFR §1.322. If any error to be corrected is the mistake of Patentee rather than the Office please treat this as a Request under 37 CFR §1.323 and charge the fee under 37 CFR §1.20(a) or any additional fees to the account of the undersigned, Deposit Account No. 23/2825. Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

Respectfully submitted,



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Docket No.: G0631.70032 US01
Date: August 11, 2005
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AUG 18 2005

(Also Form PTO-1050)

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

PATENT NO. : 6,924,759 B2
DATED : August 2, 2005
INVENTOR(S) : Wynne et al

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

(75) Inventors: should read:

John Wynne, Limerick (IE); Donal P. Geraghty, Limerick (IE); Albert C. O'Grady, Mungret (IE)

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PATENT NO.: US 6,924,759 B2

AUG 18 2005



US006924759B2

(12) **United States Patent**
Wynne et al.

(10) Patent No.: **US 6,924,759 B2**
(45) Date of Patent: **Aug. 2, 2005**

(54) **MULTI-CHANNEL INTEGRATED CIRCUIT COMPRISING A PLURALITY OF DACS, AND A METHOD FOR MONITORING THE OUTPUT OF THE DACS**

(75) Inventors: **John Wynne, Limerick (IR); Donal P. Geraghty, Limerick (IR); Albert C. O'Grady, Mungret (IR)**

(73) Assignee: **Analog Devices, Inc., Norwood, MA (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 60 days.

(21) Appl. No.: **10/731,334**

(22) Filed: **Dec. 9, 2003**

(65) **Prior Publication Data**

US 2004/0113177 A1 Jun. 17, 2004

Related U.S. Application Data

(60) Provisional application No. 60/431,909, filed on Dec. 9, 2002.

(51) Int. Cl.⁷ **H03M 1/66**

(52) U.S. Cl. **341/144; 341/143; 341/136**

(58) Field of Search **341/144, 143, 341/136**

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* cited by examiner

Primary Examiner—Don Le

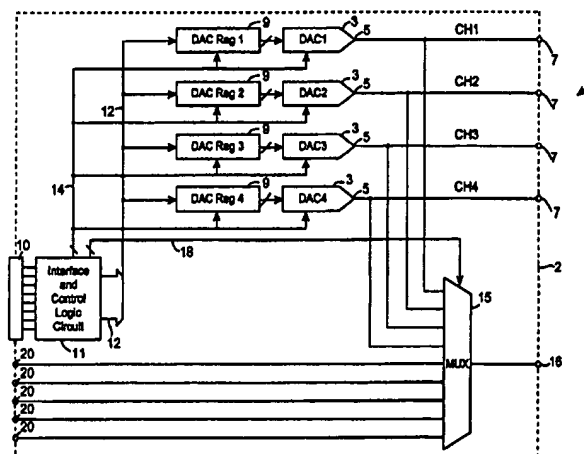
Assistant Examiner—Lam T. Mai

(74) Attorney, Agent, or Firm—Wolf, Greenfield & Sacks, P.C.

(57) **ABSTRACT**

A multi-channel circuit (1) comprising a plurality of on-chip channels (CH1 to CH4), each of which comprises a DAC (3) for converting digital data into analogue output signals independently of each other under the control of an interface and control logic circuit (11). The analogue output signals from the DACs (3) are outputted on output terminals (7) of the respective channels (CH1 to CH4). The digital input data and control and address signals for controlling the conversion of the digital data in the DACs (3) are inputted to the interface and control logic circuit (11) through an I/O port (10). DAC registers (9) are provided in the respective channels (CH1 to CH4) for storing the digital words to be converted in the corresponding DACs (3). Analogue input terminals (20) are provided for receiving analogue input signals (20), for example, analogue signals from external systems which may be controlled by the output signals from the DACs (3). A multiplexer (15) is operable under the control of the interface and control logic circuit (11) for selectively and sequentially applying the analogue output signals from the DACs (3) and the analogue input signals from the analogue input terminals (20) to a monitoring output terminal (16) for facilitating independent monitoring of the analogue output signals from the DACs (3), and the analogue inputs on the analogue input terminals (20).

21 Claims, 2 Drawing Sheets



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